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SOI CMOS For High Temperature Analog and Mixed-Signal Applications

NASA/JPL Workshop on Extreme Environments Technologies for Space Exploration

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Outline

- Honeywell DSES Markets and Products
- Markets and applications for high temperature electronics
- SOI technology for high temperature electronics (200°C to 300°C)
  - Advantages/Features for HT analog/mixed-signal applications
  - High temperature issues and mitigation approaches
  - SOI design considerations for high temp.
- Honeywell commercial high-temp. status
- Technology trends and program opportunities
- Summary

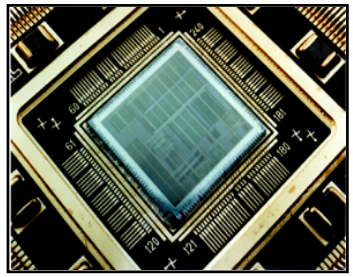
MARKETS AND PRODUCTS

Microelectronic Solutions

Integrated Sensors & Control Electronics

Aerospace

Commercial



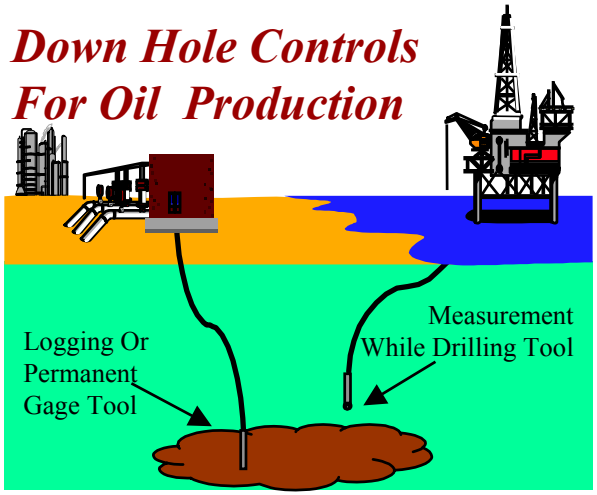
High Temp

Sensors

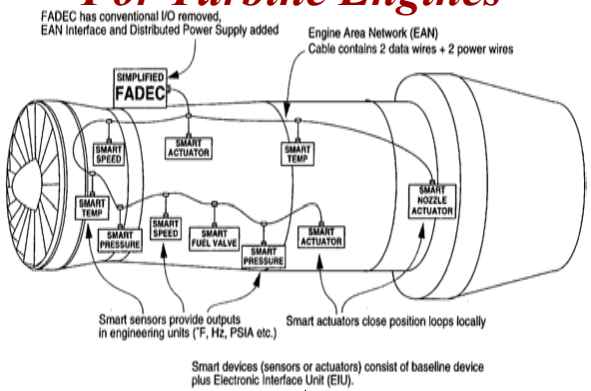
	Aerospace	Commercial	High Temp	Sensors
Markets	• Space Systems • Tactical and Strategic Missiles • Tactical Aircraft	• Industrial • Medical • Avionics • Wireless • Info Security	• Oil Service Industry • Industrial Controls • Gas Turbine Controls • Automotive	• Industrial Controls • Instrumentation • Presence Detection • Position Detection
Products	• Gate Arrays • SRAM & ROM • Bus Interface IC's • Nonvolatile Memory	• Custom Digital and Mixed Signal ASICs • Low Power ASICs • Nonvolatile Memory	• Digital and Analog ICs for Distributed Control • Pressure Transducers • Magnetic Sensors	• Pressure Transducers • Pressure Sensors • Magnetometers • Magnetic Sensors
Customers	• OEM's	• OEM's	• OEM's • End Users	• OEM's • End Users

Complete High Temperature Solutions For

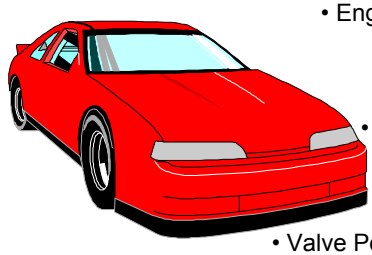
Down Hole Controls For Oil Production



Distributed Controls For Turbine Engines



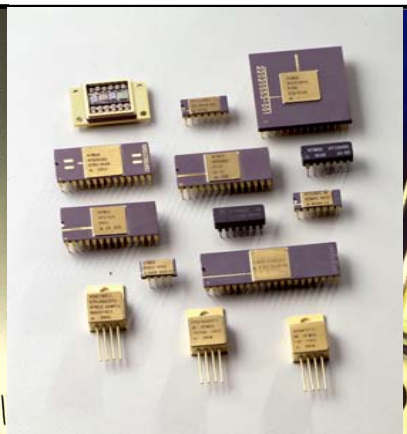
Powertrain Controls For Internal Combustion Engines

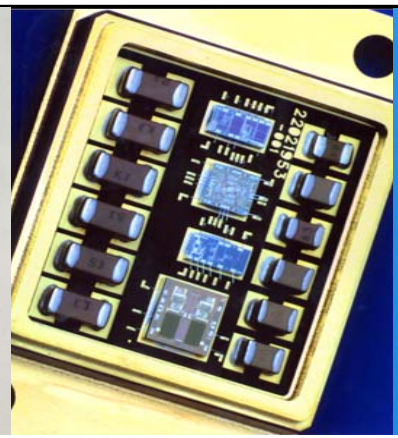


- Engine Control Modules
- Electronic Throttle
- Electronic Alternator
- Valve Actuators
- Valve Position Measurement
- Transmission Control Modules

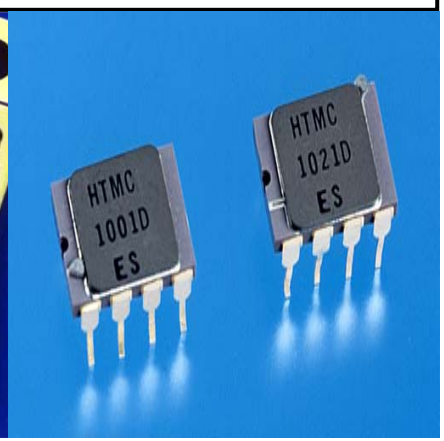
Guaranteed Operation To 225C For Five Years

Pressure Transducers





HTMOS™ Electronics And Multi-Chip Modules



Magnetic Sensors

High-temp. Market Segments

Down-hole (fossil fuel/geothermal)

- "Short life" applications
  - Measurement while drilling, data-logging
- Long-life applications (permanent installation)
  - Production management, well completions
- Temperature needs:
  - Fossil fuel: historically 175°C peak, but trending to 250°C as wells go deeper
  - Geothermal: 300 °C (and higher?)

Aerospace

- Distributed control systems
- Turbine engine sensor and control systems
- Temperature:
  - Continuum: Most applications at 200 °C or lower. A few higher than 400 °C .
  - Operating temperatures often not as high. Peak temperatures often just after engine is turned off ("soak back")

High-temp. Market Segments

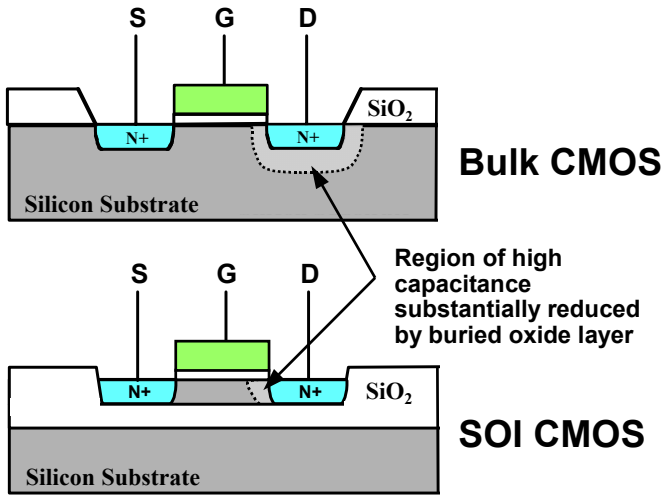
Automotive

- Engine compartment, exhaust, braking systems
- High volume, competitive, very cost sensitive
- Not many applications above 150°C to 175°C

Industrial

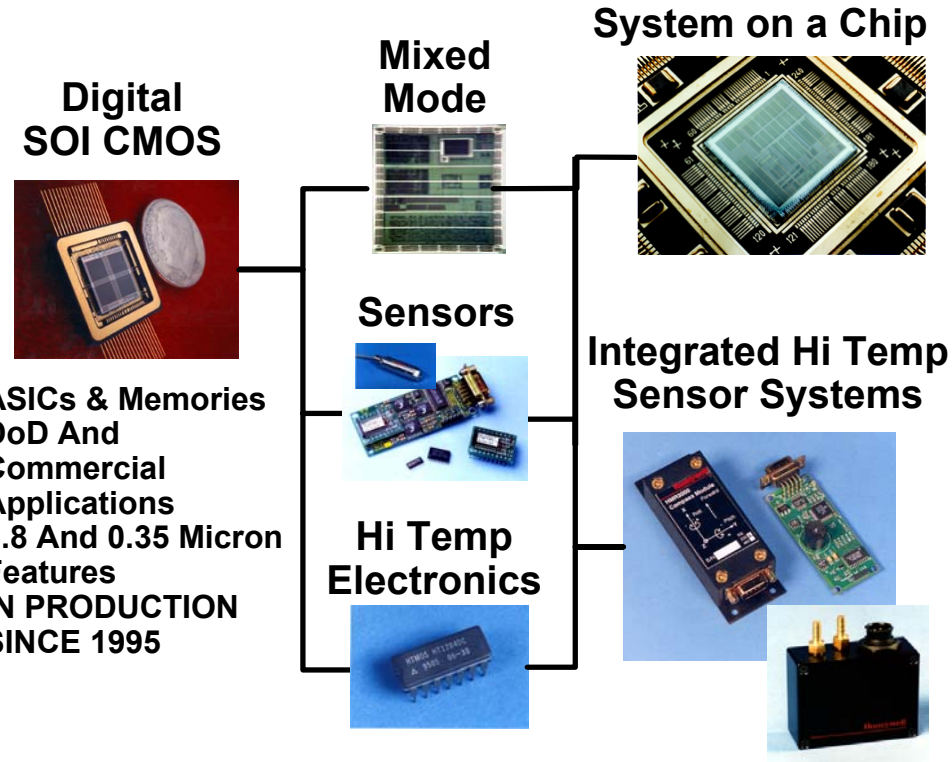
- Process controls (sensors and signal conditioning)
- Motor controls (high power density)

SILICON ON INSULATOR TECHNOLOGY

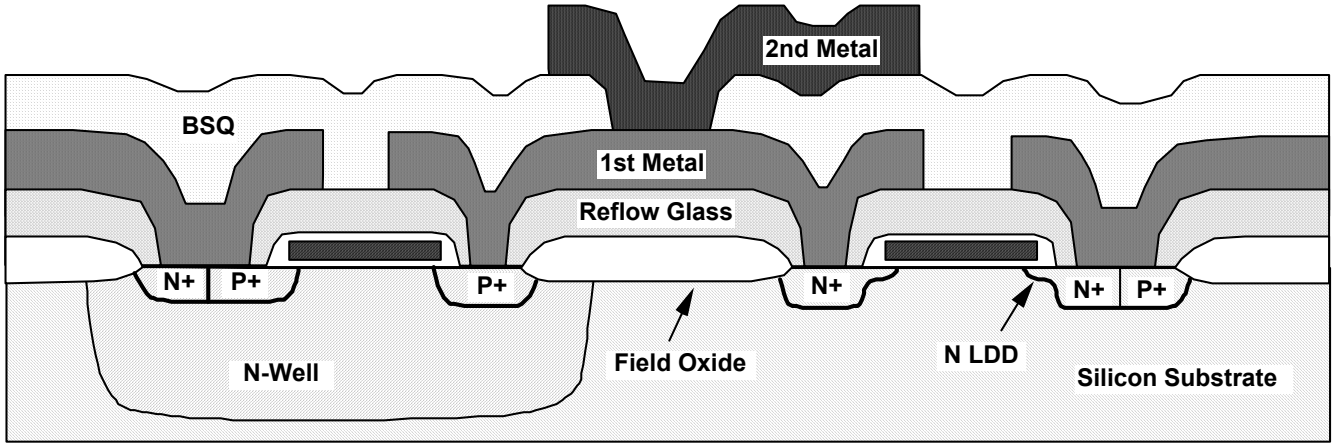


Buried SiO_2 Insulating Layer Provides The Following Benefits

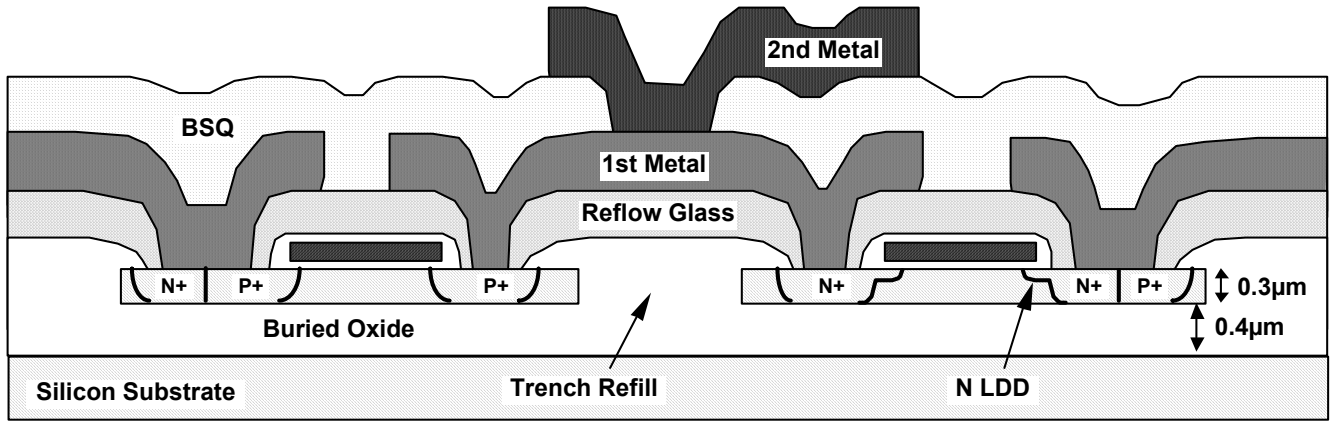
- 30% To 40% Faster Circuits
- 30% To 40% Lower Power
- Better Isolation For Mixed Signal ASICs
- High Reliability – No latch-up
- High Temperature Operation : 225°C continuous and excursions to 300°C
- Improved Sensor Accuracy And Stability



Bulk Vs. SOI Cross-Section



Bulk



SOI

Honeywell High-temp. SOI Process Options

	"10V Linear" Process	SOI4 High Temp. Process
Gate Oxide	350 angstroms	150 angstroms
Max. Gate Ox. Voltage	10V	5v
Target Vtn/Vtp	1.2V / -1.2V	1.2V / -1.3V
Min transistor length	1.2 microns	0.8 microns
# of metal layers	2	3 or 4
Top Si Thickness	0.3 microns	0.3 microns
Buried Oxide	1.0 micron	0.4 microns
Partially/Fully depleted	Partially depleted	Partially depleted
Lithography	1X	5X
DMOS option	Yes: >30V VDS	Yes: >20V VDS
CrSiN resistors	Yes	Yes
Linear Cap Implant	Yes	Yes
Laser trim fuse links	Yes	Yes
Lateral PNP VREF	Yes	Yes

SOI4 High-Temp. is identical to radiation-hardened SOI4 except for target Vt and non-hardened oxides

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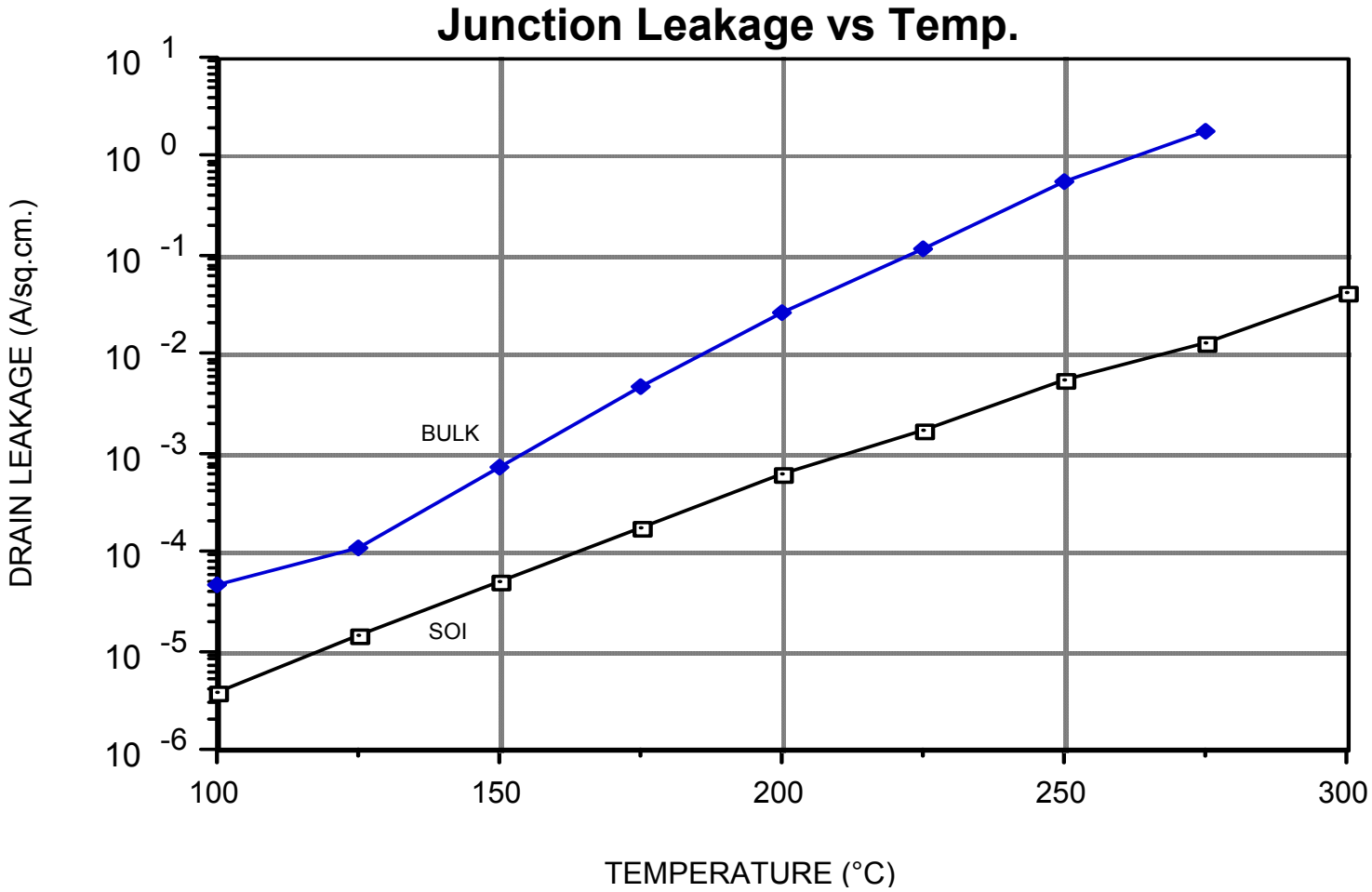
SOI vs. Bulk Leakage and Delay (1.2μ Process)



SOI has >10x <u>less</u> leakage than Bulk

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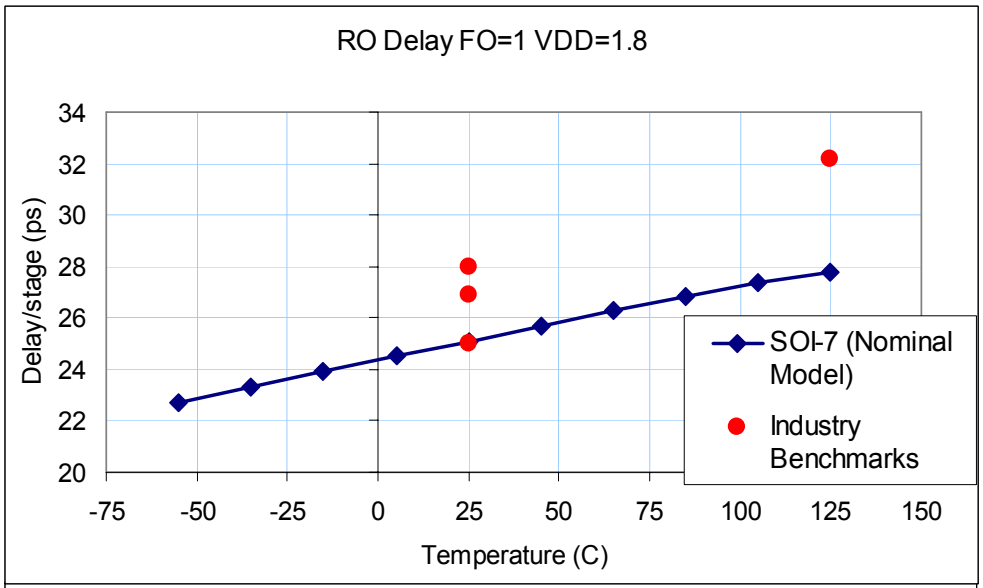
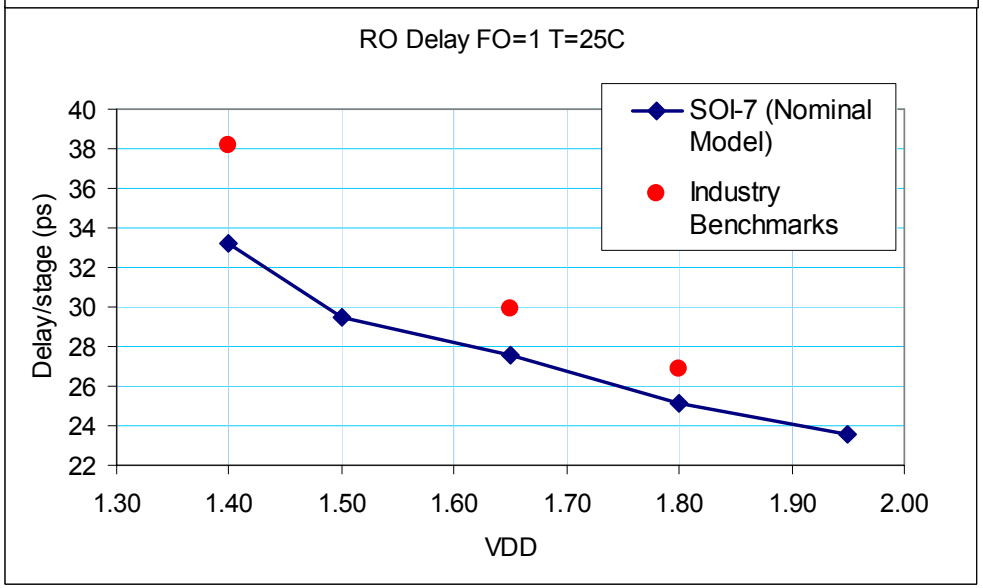
Ring Osc. Performance – 1.8V Benchmarking





Gate Delay Predictions

SOI-7 Nominal Model versus 1.8V bulk CMOS

The SOI-7 performance predictions are better than the 1.8V industry benchmarks over the full temperature range of –55C to +125C.

Performance over voltage is better than 1.8V industry benchmarks. A 18% increase in gate delay is predicted when the supply voltage is reduced from 1.8 to 1.5 volts

SOI-7 provides better performance than 1.8V industry benchmarks because of the intrinsic speed advantage of SOI

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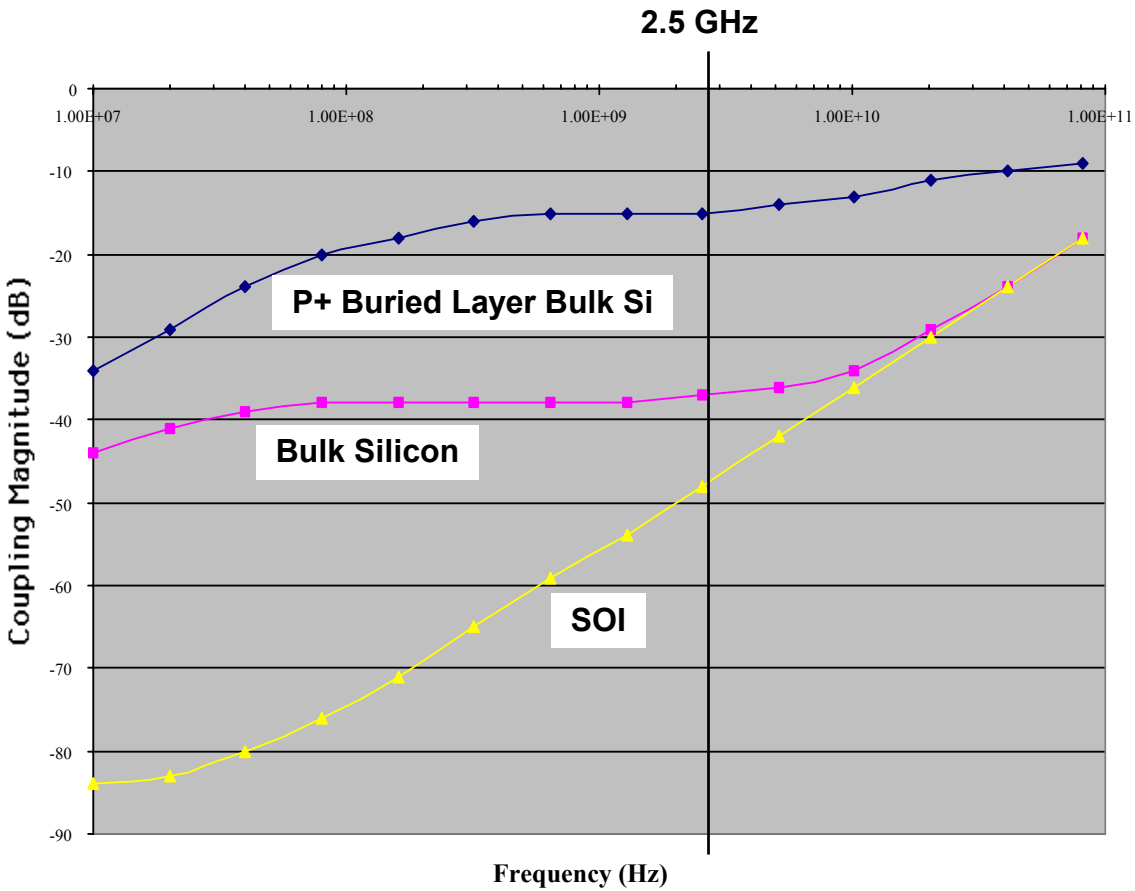
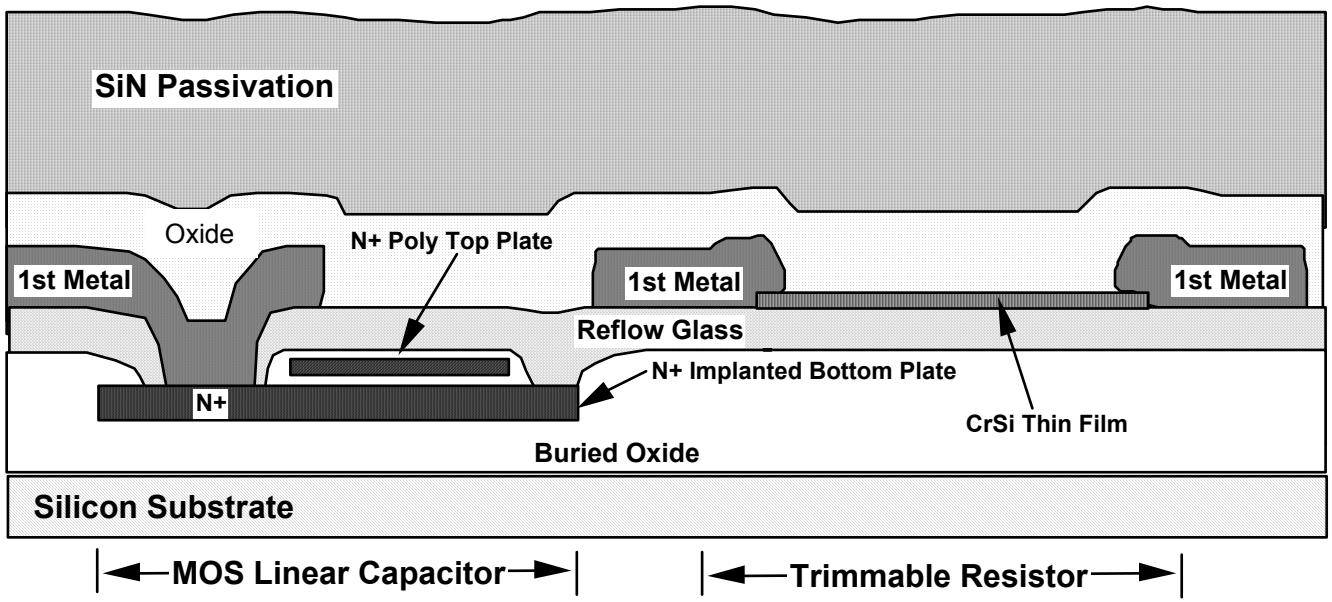
SOI CMOS is a Good Substrate Solution for Mixed Signal Applications



***SOI Advantages*:**

- **10 –30 dB less coupling between analog and digital circuits measured at 2.5 GHz**
- **20 – 30 % Lower Power Circuits Bulk CMOS**
- **Radiation Hardened**

Capacitor / Resistor Cross-section



- N+ poly to N+ Si capacitor
  - Special implant for capacitor bottom plate
  - 700Å oxide dielectric, 0.5fF per sq. micron
  - Less than 150ppm/V, 20ppm/°C
- Laser-trimmable CrSi thin-film resistors
  - Direct 1st metal contactless interconnect
  - 2500Ω/sq, less than 300ppm/°C

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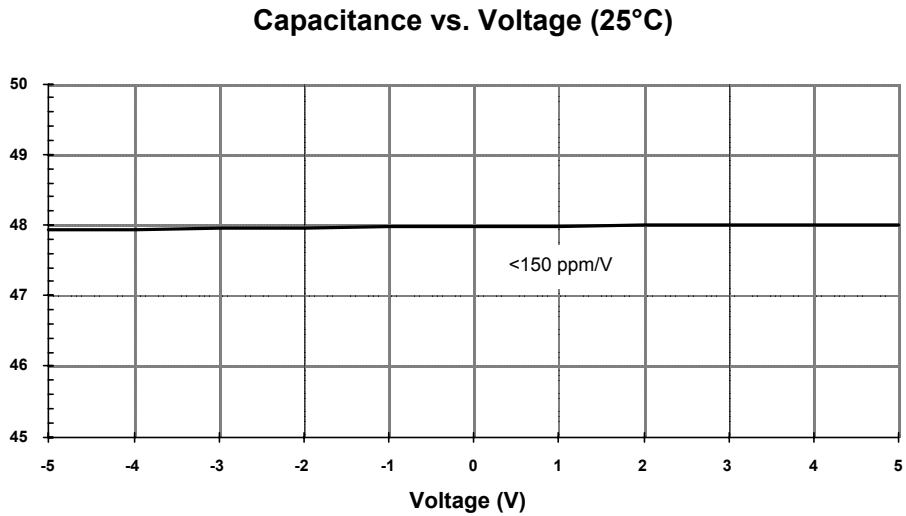
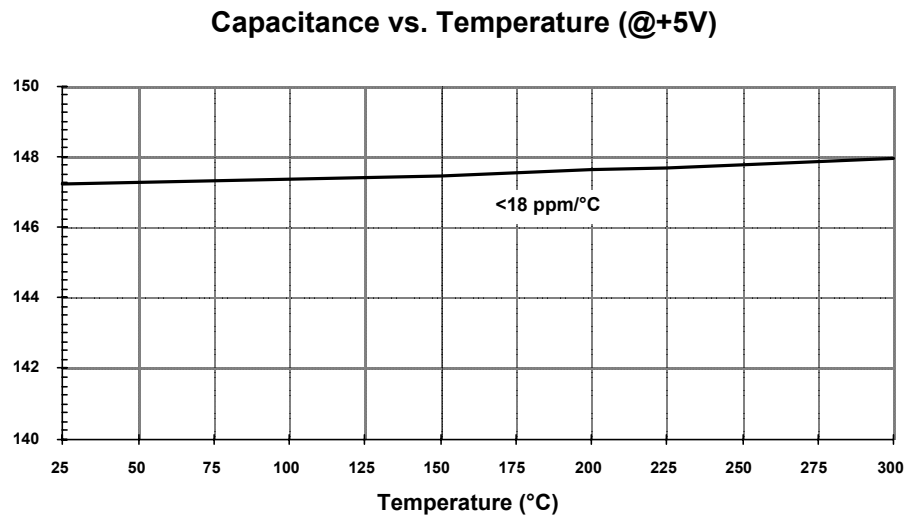
Linear Capacitor Coefficients



Voltage Coefficient

<150 ppm/V



Temperature Coefficient

<18 ppm/°C

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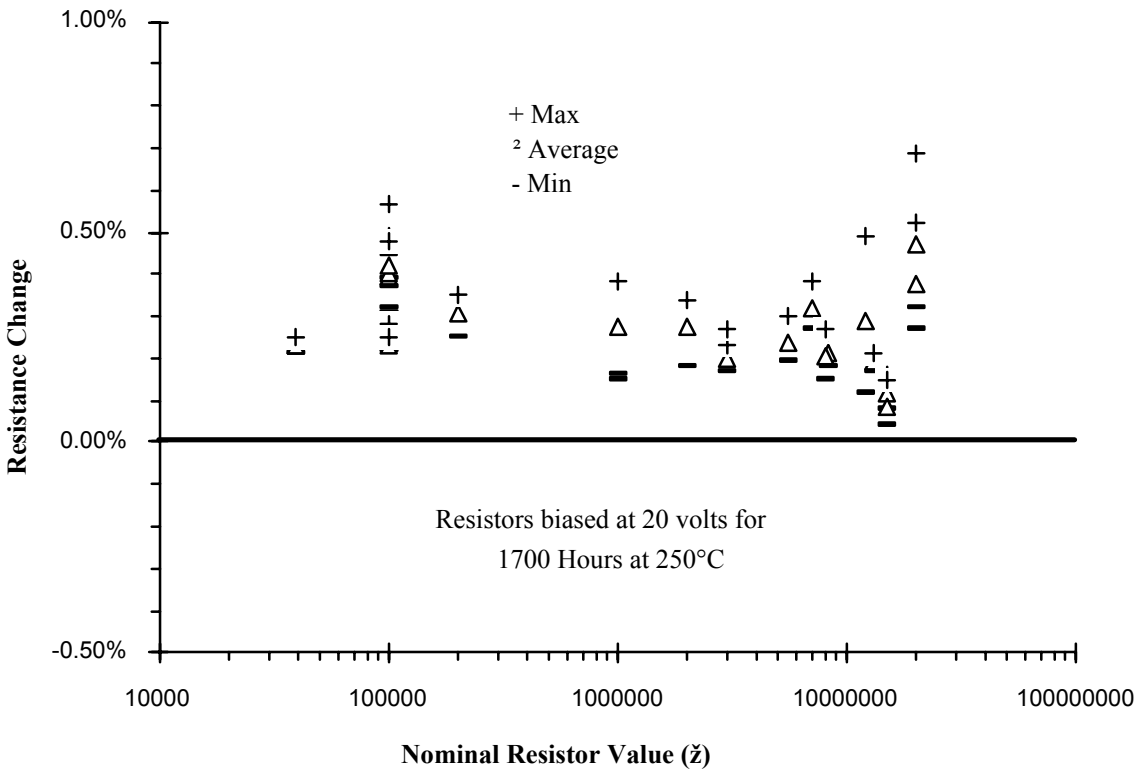
Thin Film Resistor Characteristics

- Low risk, mature technology
- High sheet rho (2500Ω/sq.), large value resistors possible
- Low TCR (±300ppm/°C max, ±200ppm/°C typ.)
- Good matching (0.1% ratio match, untrimmed*)
- Less than 5ppm/°C typical TCR match
- Stability, high temp. capability demonstrated (250°C)

Thin-Film Resistor Stability

Resistance Change From Time=0.
Measured At 200°C After 1700 Hours Biased @ 20V, 250°C



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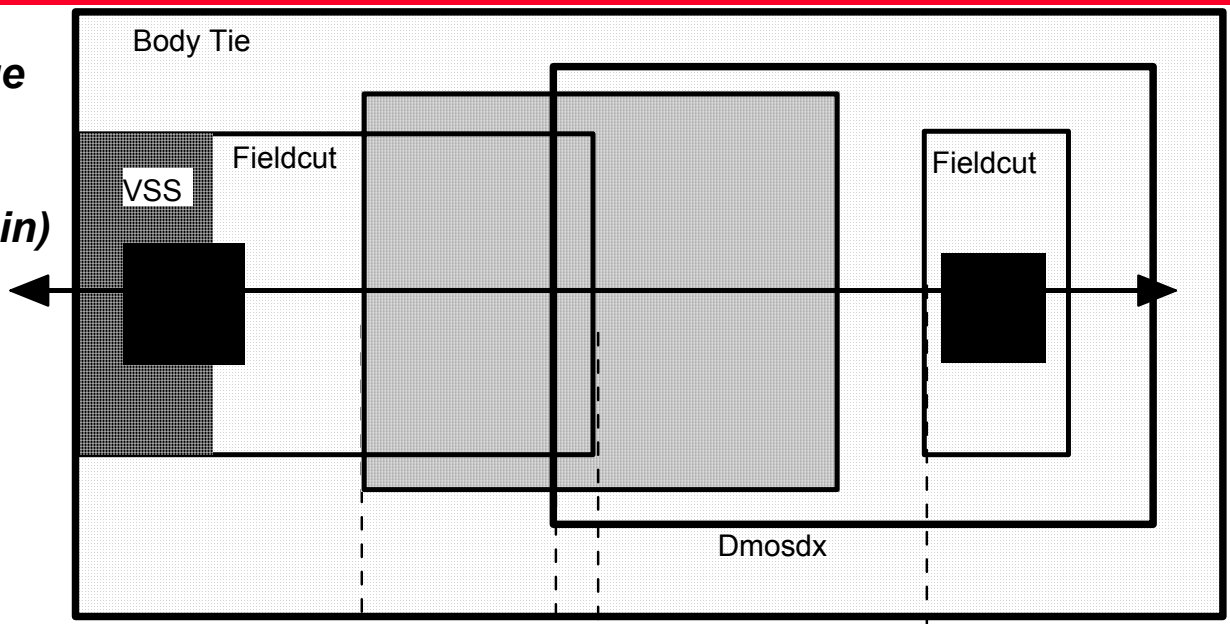
SOI4 Nch DMOS Layout Approach

Increased Drain-Source Voltage

Reduce drain conductance in saturation (high DC voltage gain)



Dimension A

- **Gate Length (source edge defined by poly, drain edge by field cut).**

Dimension B

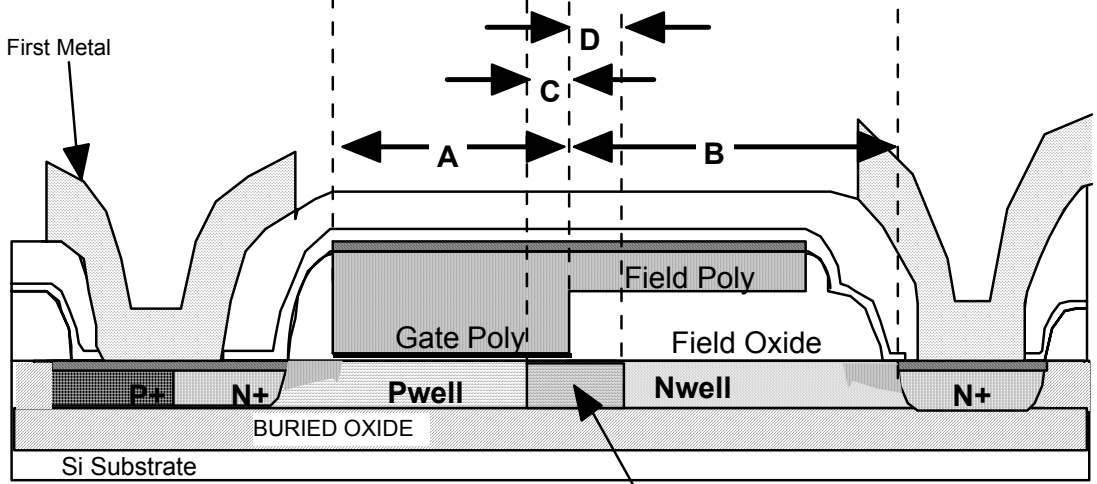
- **Drain Extension (Fieldcut edge to Fieldcut edge).**

Dimension C

- **Drain extension under Gate Oxide (Dmosdx edge to source fieldcut edge).**

Dimension D

- **Nwell / Pwell overlap (from Dmosdx layer by sizing/mask generation.**



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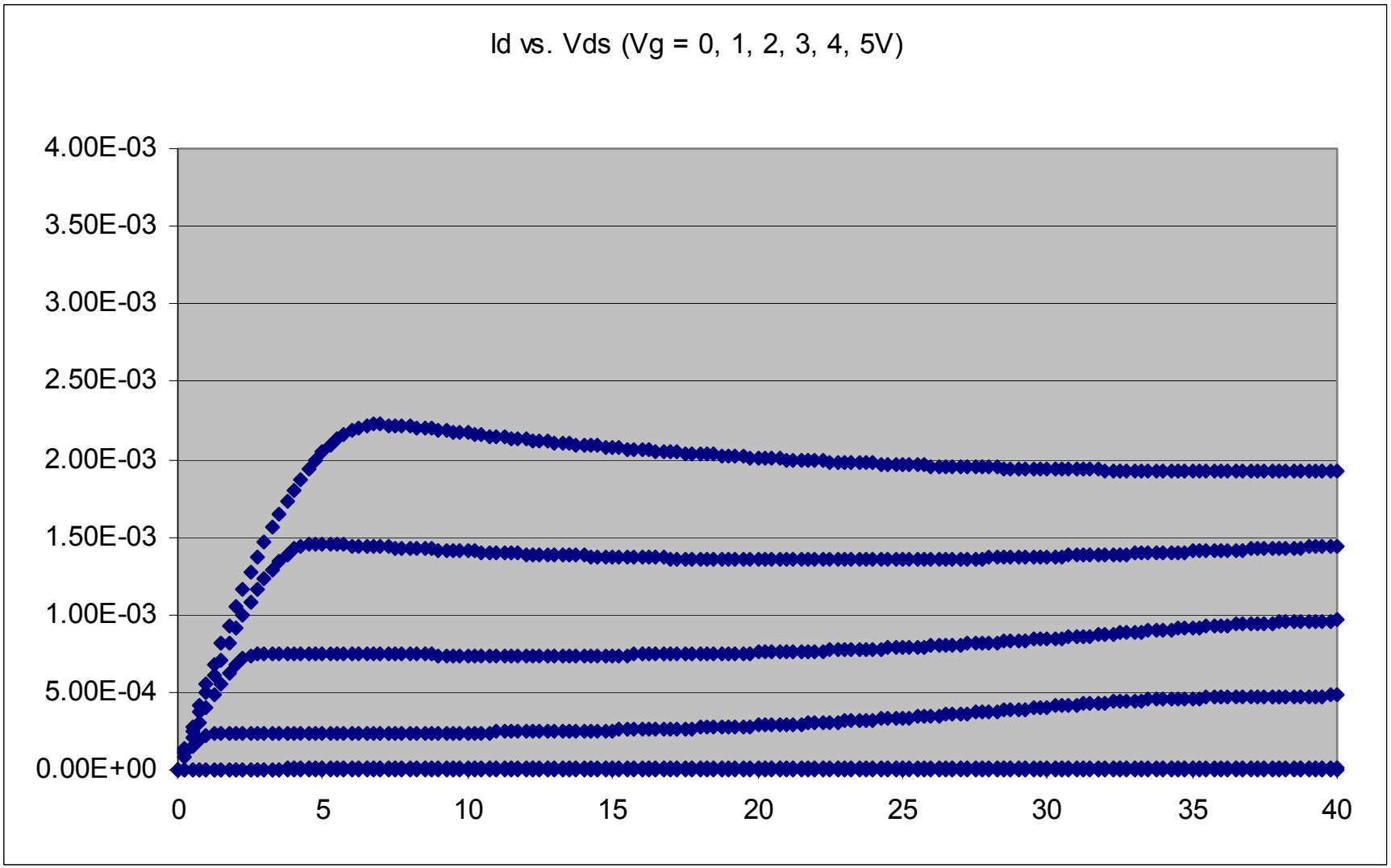
SOI4 Nch DMOS Transistor I-V Characteristic



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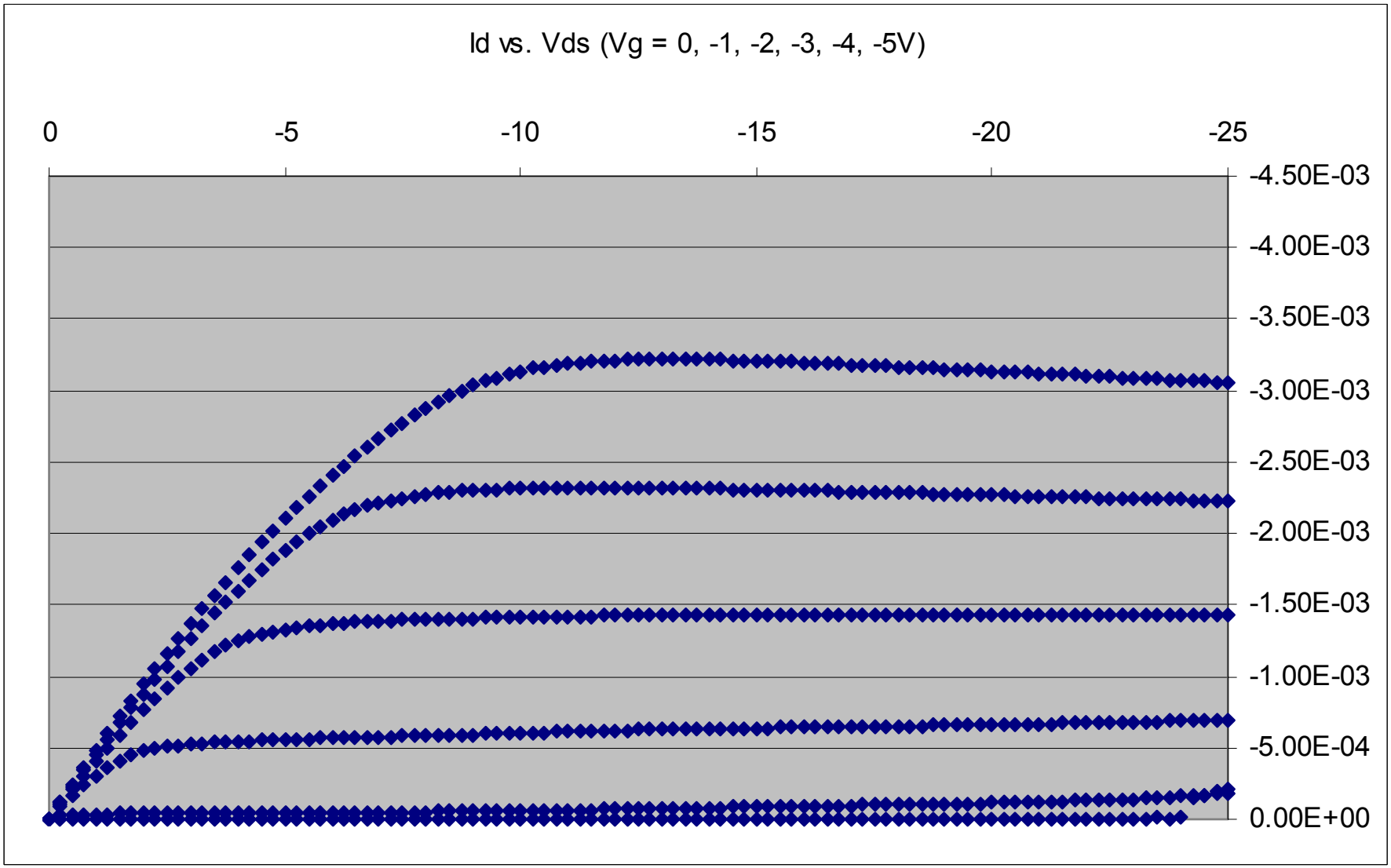
SOI4 Pch DMOS Transistor I-V Characteristic



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High-temp. Issues & Mitigation Approaches

Junction Leakage

- Junction leakage doubles every 10°C (above ≈170°C)
- Use SOI processes – full oxide isolation

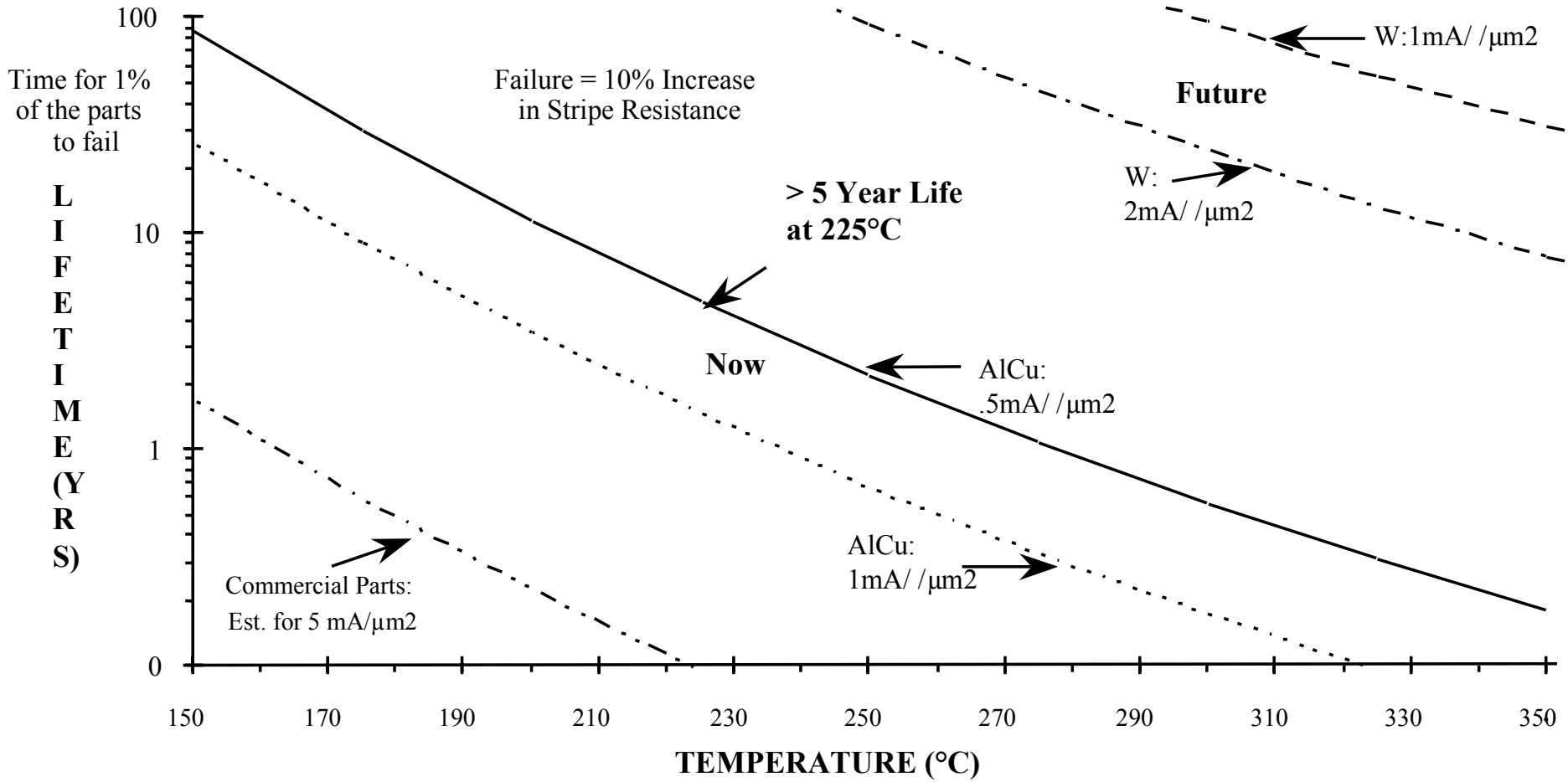
Sub-threshold transistor leakage

- Threshold voltage has a negative temperature coefficient typically – 2mV/°C. Standard SOI processes leak badly above 200°C due to sub-threshold conduction.
- Re-target room-temp. Vt's to compensate
  - Trade-off vs. drive current, voltage head-room.
  - One reason why 5V process persists for HT vs. 3.3, 2.5, 1.8.

Electro-migration

- Aluminum inter-connect migration exponentially related to temperature
- Design to more conservative design rules
  - Wider metal traces / more vias and contacts
  - OR reduce the operating frequency (digital circuits)
- OR develop alternative inter-connect metalization (e.g., Tungsten)

Electro-Migration Lifetime vs. Current Density



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High-temp. Issues & Mitigation Approaches

Reduced mobility vs. Temperature

- Reduces digital drive currents, analog gain (gm)
- Use larger devices for digital logic (or de-rate speed at HT)
- Temperature compensate bias currents to stabliize gain vs. temp. (increases power consumption at high temp.)

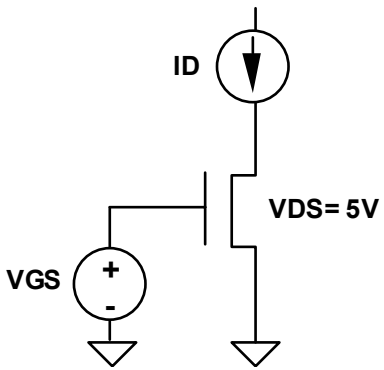
Bias voltage drift with temperature

- Mobility and Vt drift with temperature may cause wide range of bias voltage variation, eating into common-mode input range or output range
- Use “Zero Temperature Coefficient” biasing
  - Play Vt shift against mobility shift to stabilize bias voltages
  - Requires good models over temp.

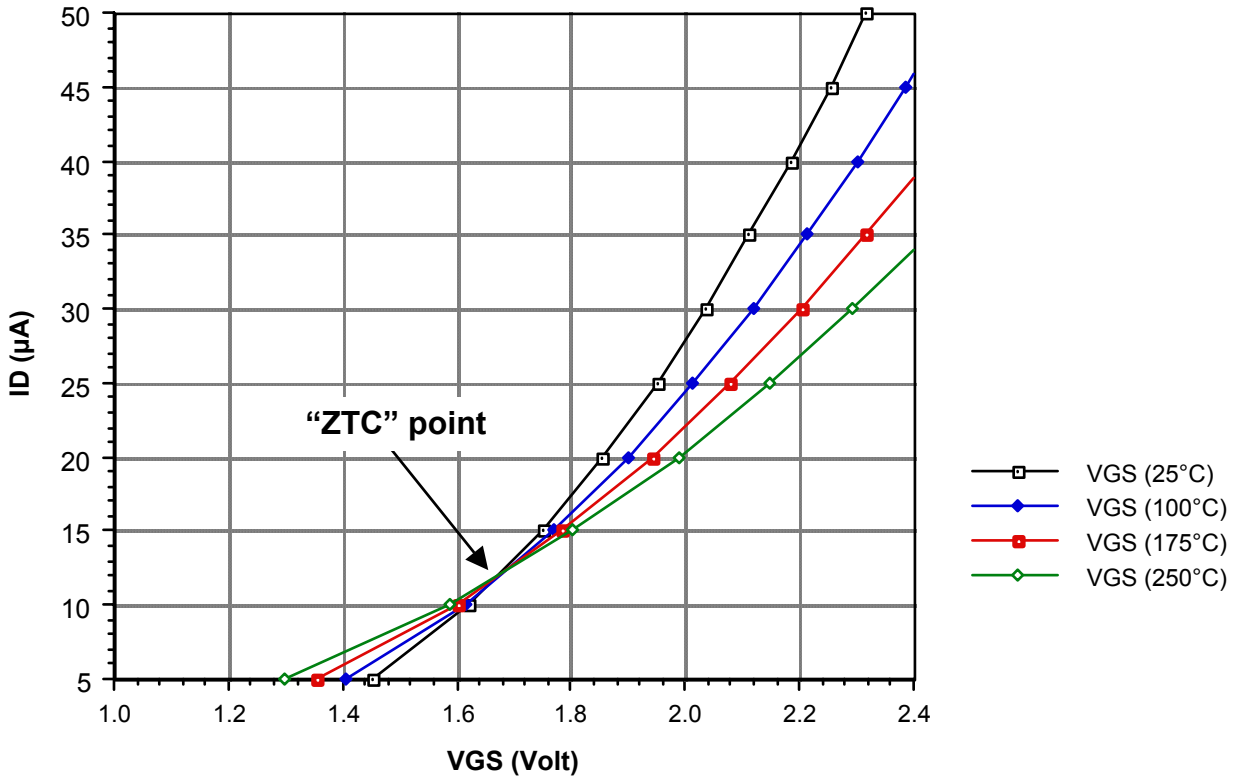
Zero Temperature Coeffiicient Biasing

Circuit Applications

- Current Source
- Current Mirrors
- Differential Inputs



15/10 N-channel



SOI Issues

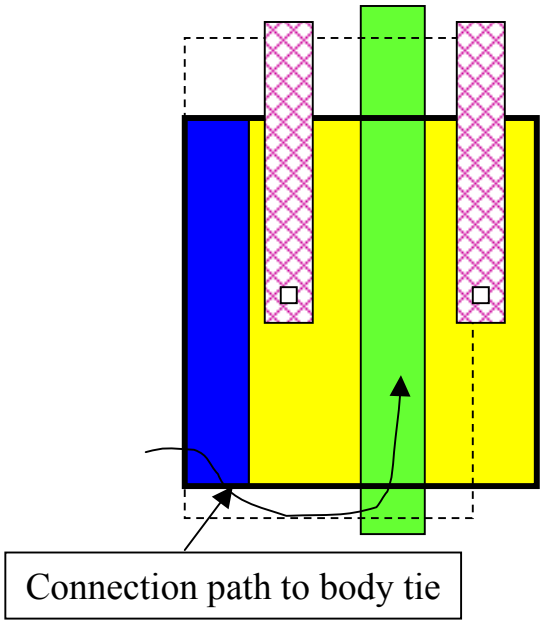
Self-heating

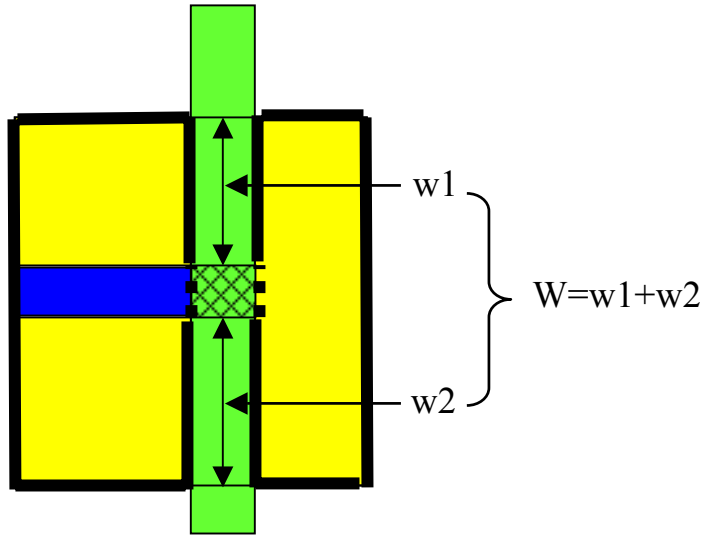
- SOI thermally isolates devices, resulting in localized self-heating when the power density is too high.
  - Impacts high-speed, high-drive analog/digital, output drivers
  - Mitigate by designing for lower current density.
  - Intelligent system partitioning
    - SiC power devices are inherently more capable than Soi

Floating Body Effects

- Fully-depleted SOI has no body tie
  - Subject to “kink” effects, problems with total dose environments
- Partially-depleted SOI leaves option to connect to the body-tie
  - “Floating body” option has advantages for SOME applications, but is not a good option for total dose environments or analog
  - Solution is to make explicit body connections.
  - PD-SOI body connections are resistive, and can lead to parasitic bipolar effects.
    - Multiple parameters involved, each with its own temp. variation
    - Net impacts not much worse at high temp. than conventional temp
  - Solution is characterization to develop max. device width rules.

Body Tie Options : Source-to-Body Tied MOSFETS





Note: Body tie options and the Area "cost" may vary widely among SOI manufacturers

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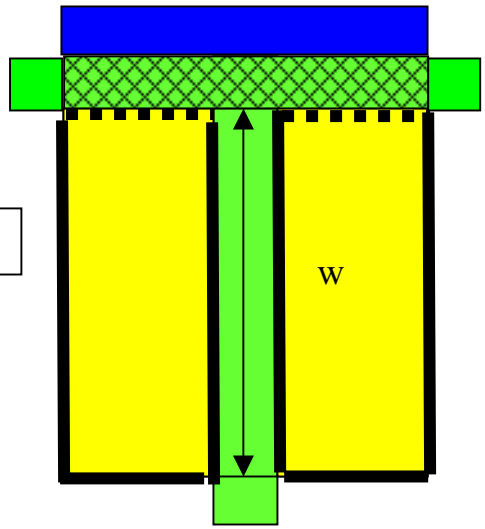
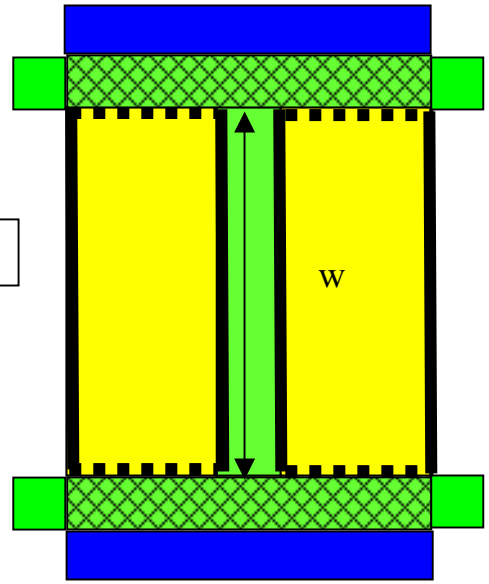
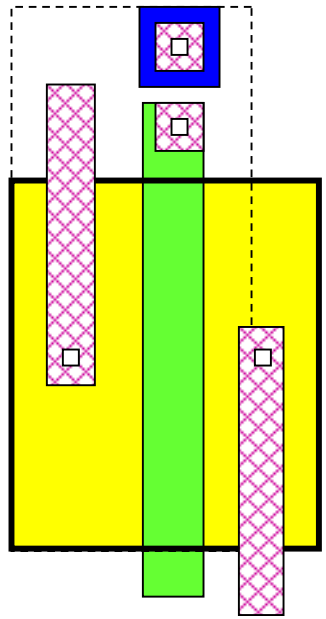
Body Tie Options for "4-terminal" MOSFETS

Tgate approach



Hgate approach





Body-tie Silicon Approach

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SOI Issues

Back-gate Transistors

- The buried oxide forms a “back-gate” transistor that may turn on depending on how the wafer substrate is biased relative to the top silicon
  - Back-gate transistor turn-on voltage varies significantly with temperature
  - Typically connect substrate to the most negative potential on-chip
  - This phenomenon limits the useful operating range for Pch DMOS transistors
  - This is one reason to use thicker buried oxide

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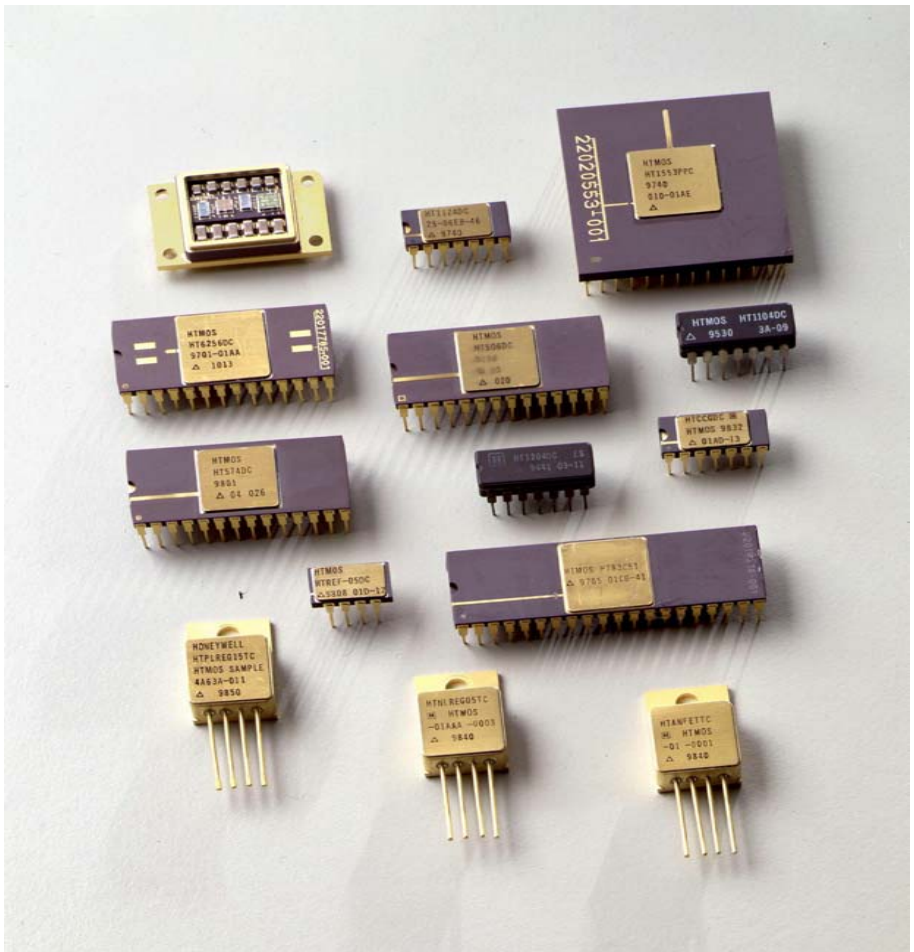
Honeywell High Temperature SOI Circuits/Devices

HTMOS™ Standard Electronic Products



- Available Now!
- Family Of SOI* CMOS Integrated Circuits For Creating Data Acquisition & Instrumentation Subsystems
  - Op Amps
  - Voltage References
  - Voltage Regulators
  - Micro Controller
  - SRAM And ROM
  - Digital Logic Arrays
- 2 Million Device Hours Worth Of Life Test Data Demonstrate Reliable Operation At 225°C

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* Silicon On Insulator

Current HTMOS Standard Electronic Products

Product #	Function	Die	SCP
HT1104	Quad Op Amp	Now	Now
HT1204	Quad Switch	Now	Now
HT506	16:1 Analog Mux	Now	Now
HT507	8:2 Analog Mux	Now	Now
HT6256	256K Bit SRAM	Now	Now
HT83C51	8 Bit Micro Controller	Now	Now
HT2080	80K Gate Digital Array	Now*	Now*
HT2160	160K Gate Digital Array	Now*	Now*
HTCCG	Crystal Clock Generator	Now	Now
HTPLREG	+5, +10 Or +15V Voltage Regulator	Now	Now
HT574	12 Bit A/D Converter	Now	Now
HTANFET	Power FET	Now	Now
HT6656	256K Bit ROM	Now	Now

Products in Red are 5V, 0.8μ SOI4 High Temp. Process

Products in Black are 1.2μ 10V-Linear High Temp. Process

SOI Example Capability vs. Temperature

10-Transistor OP-Amp Results

Data From Lot 16619-02, +/-2.5V Supplies

Sample #4	25°C	300°C
Isupply	224 µA	198 µA
Voffset	-5.3 mV	-4.55 mV
Input Bias Current*	-0.019 nA	17.3 nA
Ioffset	0.028 nA	23.1 nA
Gain	96.2 dB	87.6 dB
CMRR	75.0 dB	77.7 dB
PSRR*	65.2 dB	72.3 dB
Input Range	-1.2V to 2.1V	-1.3V to 2.0V

* Worst Case of plus/minus bias current and power-supply rejection
Data collected for 20 pF capacitive load

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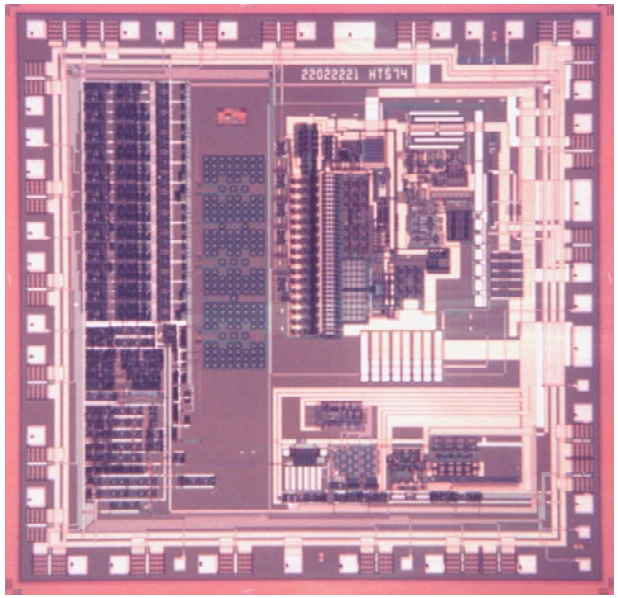
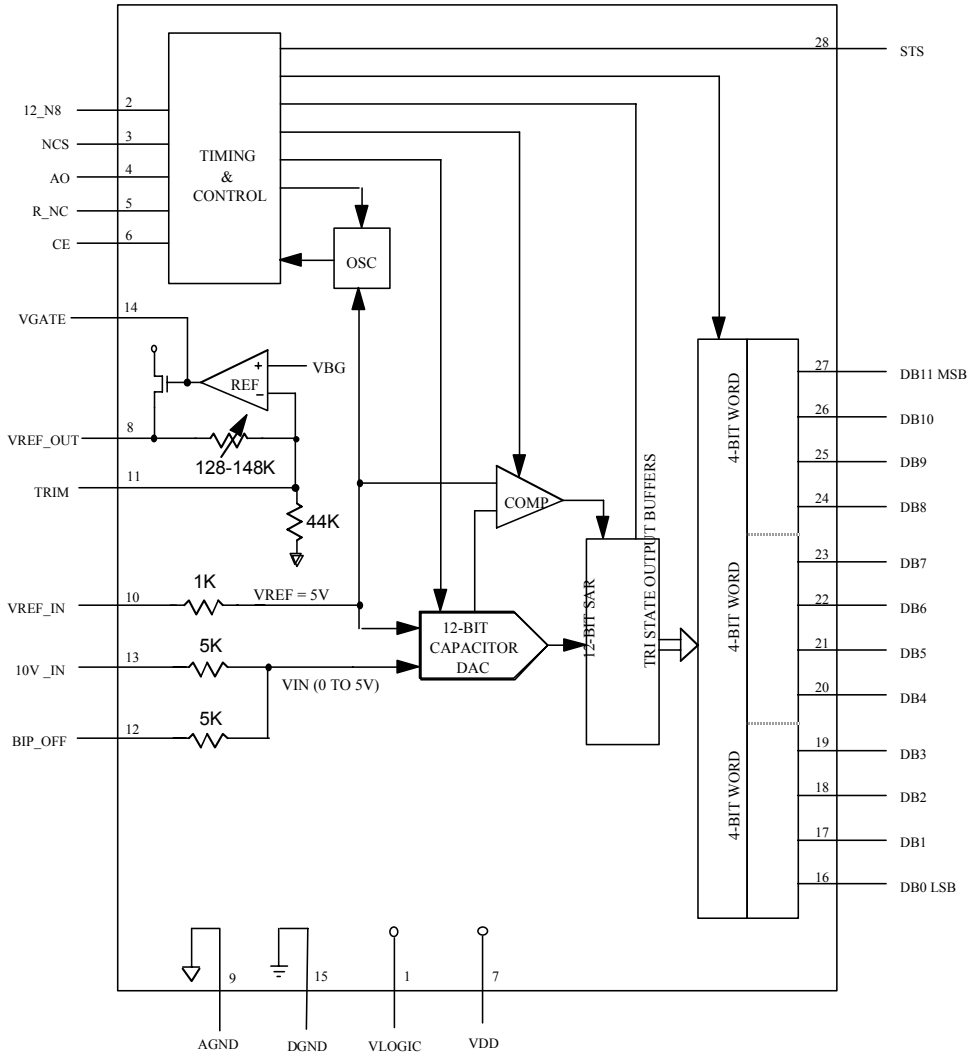
HT574 High Temp. 12-bit A/D



PARAMETER	GOAL	STATUS
Operating Temperature	-55°C to 225°C	Verified (A/D operation to 275°C)
Integral Non-Linearity	±1LSB	±1.5 LSB
Diff. Non-Linearity	±1LSB	±1 LSB, Monotonic
Offset Error	±2LSB's	+1 LSB (typical)
F.S. Calibration Error	0.8 % of FS (typical)	Verified
PSRR (10V ±1V)	±2 LSBs	±1LSB Verified
Operating Currents: VDD/Vlogic (10V/5V)	2mA/200µA	1.3mA/0.5mA (typical)
Conversion cycle	<32µsec	30µsec (typical)
Conversion cycle change, -55°C to 225°C		<3%
Vref Out @ 25°C	5V± 0.025V	Verified
Vref Out drift w/Temp.	±25mV (full range)	Verified
Vref Out drift/time	±3mV/1000 hrs	Verified
Vref Out regulation	<1mV/Volt	Verified



All devices receive 2-week dynamic burn-in @225°C prior to testing

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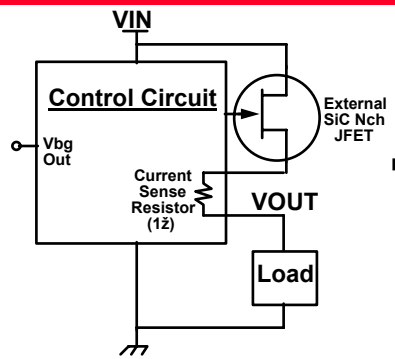
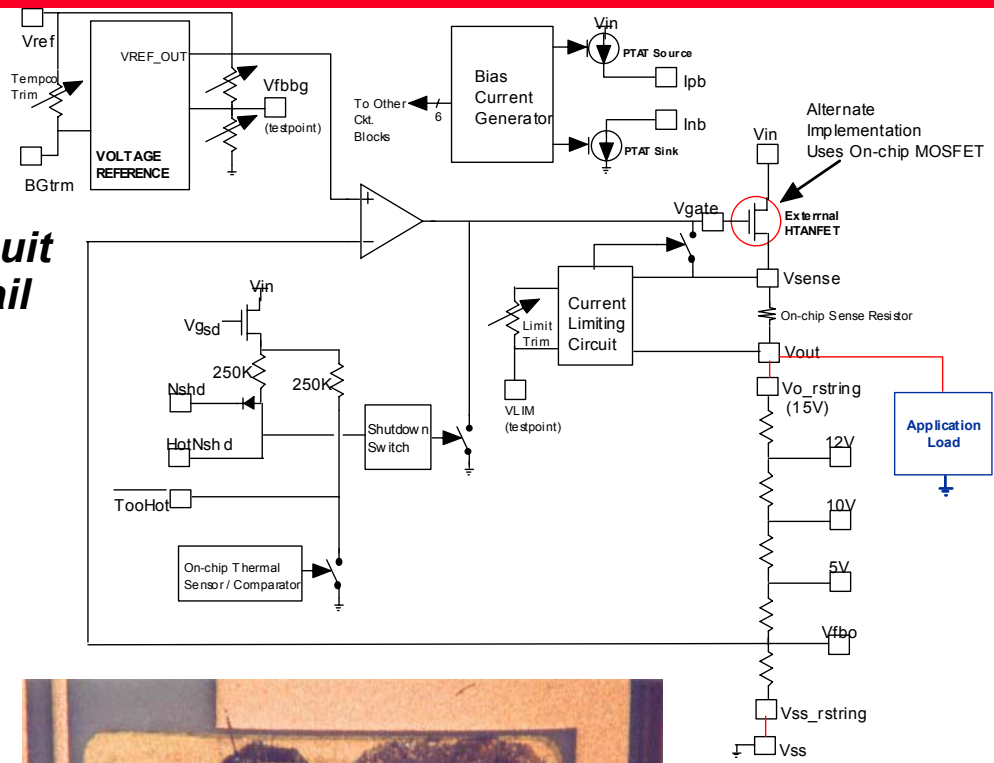
HTPLREG High Temp. Linear Regulator



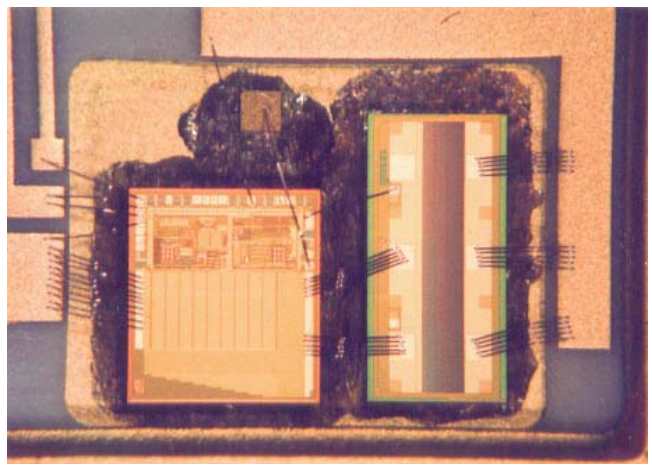
Circuit Detail



HTPLREG10 DESIGN PARAMETERS

Specified Operating Temperature Rarnge:	-55°C to 225°C (Functional with reduced performance to 300°C)
Input Voltage:	8V to 30V
Output Voltage:	5V*, 10V*, 15V*
Output Current	=0.5 amps (continuous)
Line Regulation:	±0.3%
Load Regulation:	±0.5%
Standby Current:	<1 mA (no load)
Current Limiting:	Configurable*
Power Limiting:	Configurable**
Noise (10Hz. to 10KHz) :	<2mV RMS
Input to Output Differential Voltage:	3V to 18V
External Shutdown Input:	Provided

*Configurable by wirebond at package assembly.
**Configurable by laser-trim at wafer level.



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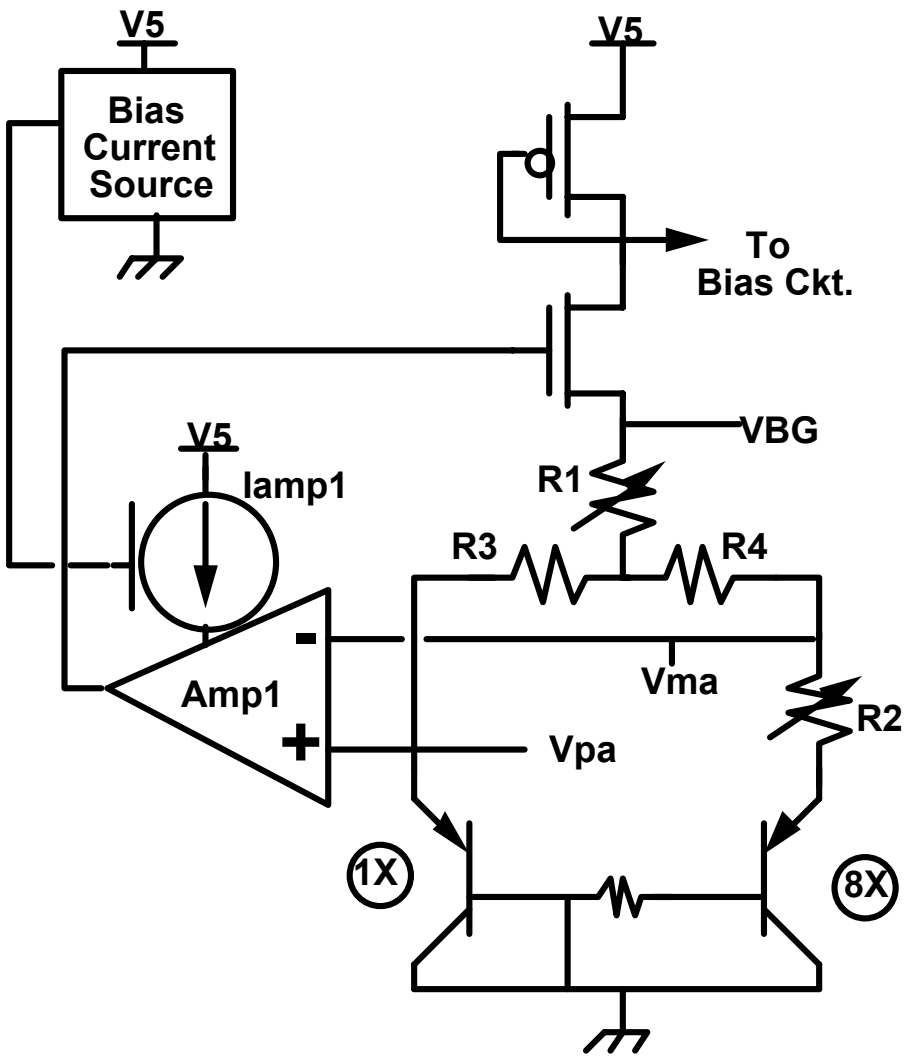
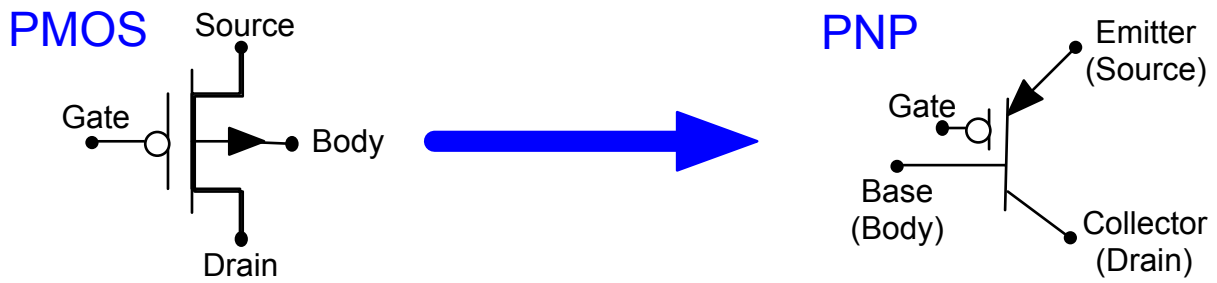
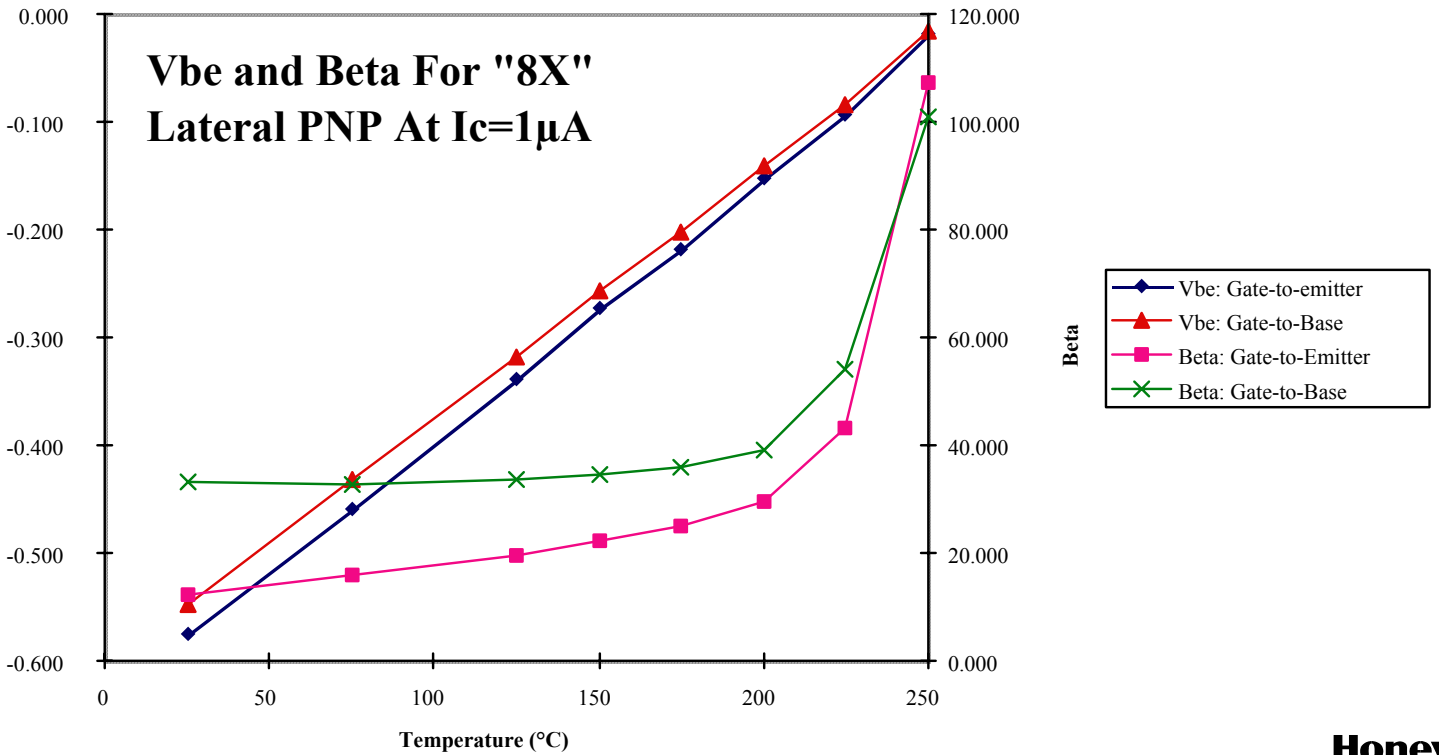
HTPLREG Bandgap VREF Block Diagram



PNP Parameters Vs. “Gate” Connection





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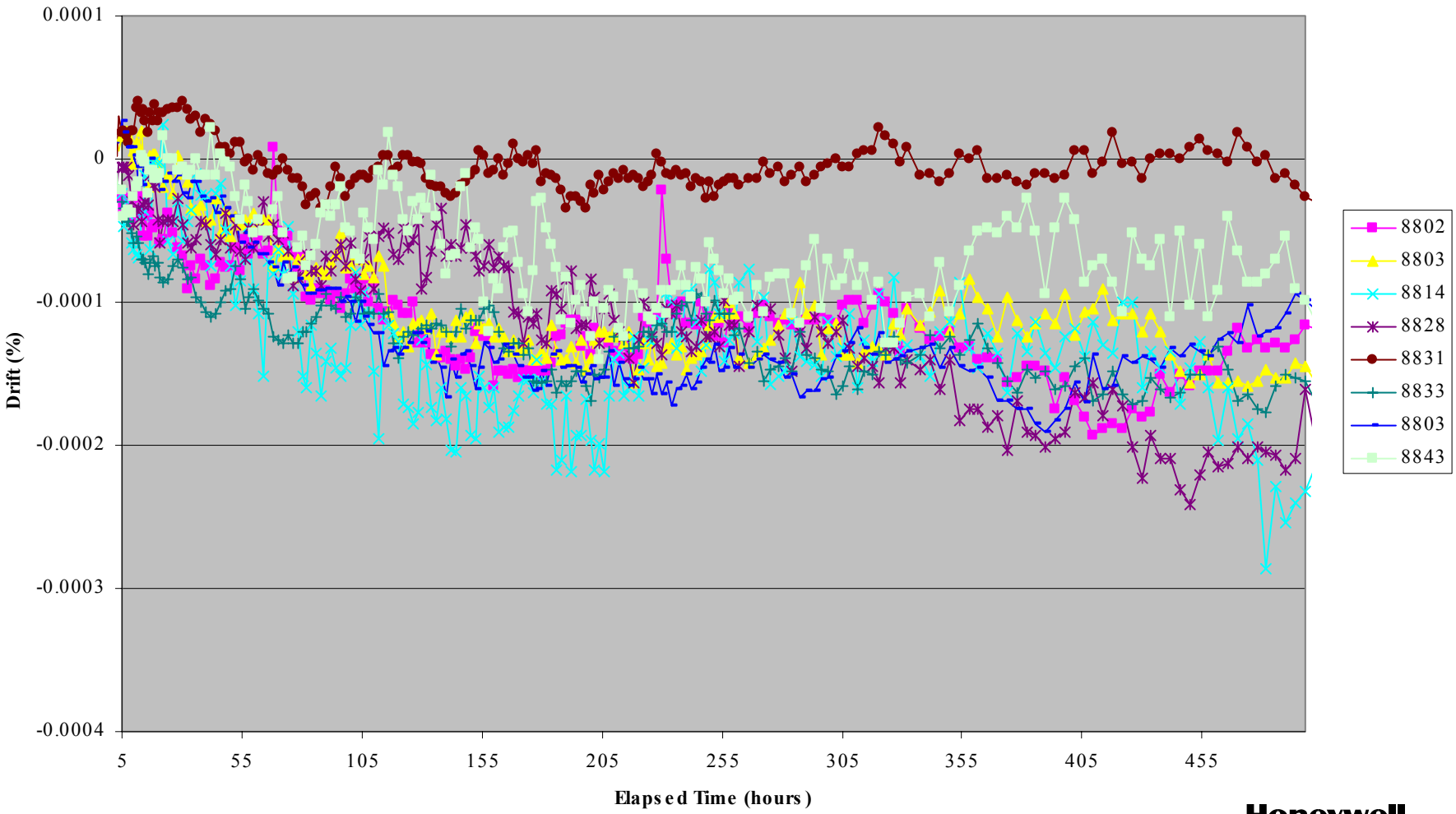
HTPLREG Output Stability

Posreg lot 2B88 samples: Drift vs. Time @ 225°C
Vin=30v, Vout=5V
Note: 0.01%= 0.5mV. Test started after burnin.



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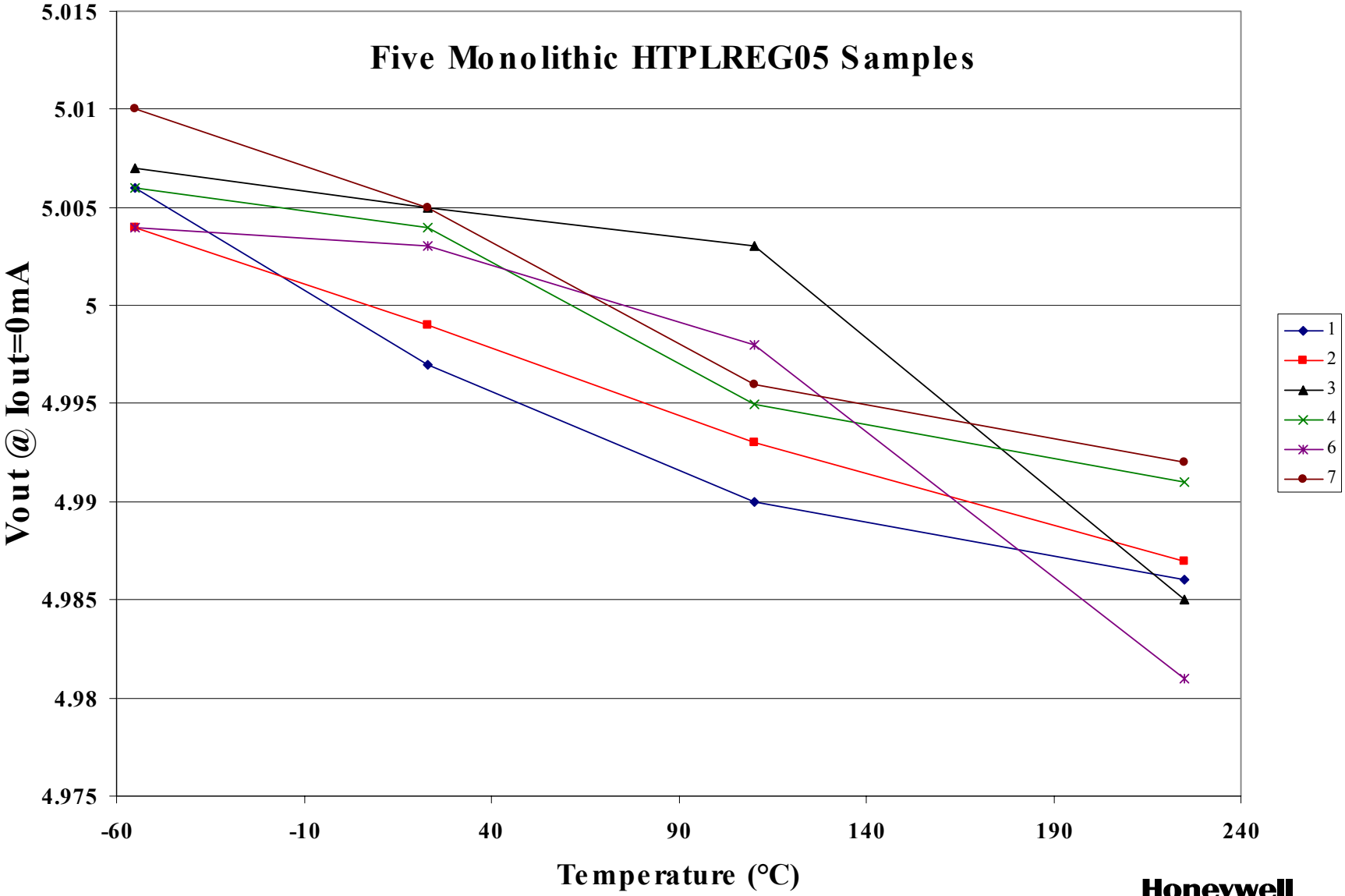
HTPLREG Output vs. Temp.



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High Temp. Supply-chain Issues

- SOI (Silicon On Insulator) Technology Is Key For High-temp applications
  - Commercially available SOI processes may not be suitable for high temp (>200°C) due to sub-threshold leakage and/or total dose response
- High Temperature Business Is Intrinsically Low-volume
  - How do we sustain commercial viability?
- Electronic Component Availability Is A Function Of The Economics For Maintaining The Manufacturing Technology
  - Commercial electronic processes are driven to smaller geometries and lower voltages by high-volume application
- Need complete electronics solution: Analog, Digital, Passives

Honeywell High Temp. Strategy

- Leverage Honeywell / U.S. DoD* support of advanced SOI technology developed for Aerospace/Defense applications
- Develop High-Temp. solutions that are derivatives of those SOI Processes, Products, and Development Platforms used to meet U.S. DoD military/strategic requirements
- Win U.S. Dept. of Energy Deep Trek program funding to accomplish this (Q3 ’03)
- No new development in “10V Linear” SOI process

*DoD = Department Of Defense

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U.S. DoD Synergy

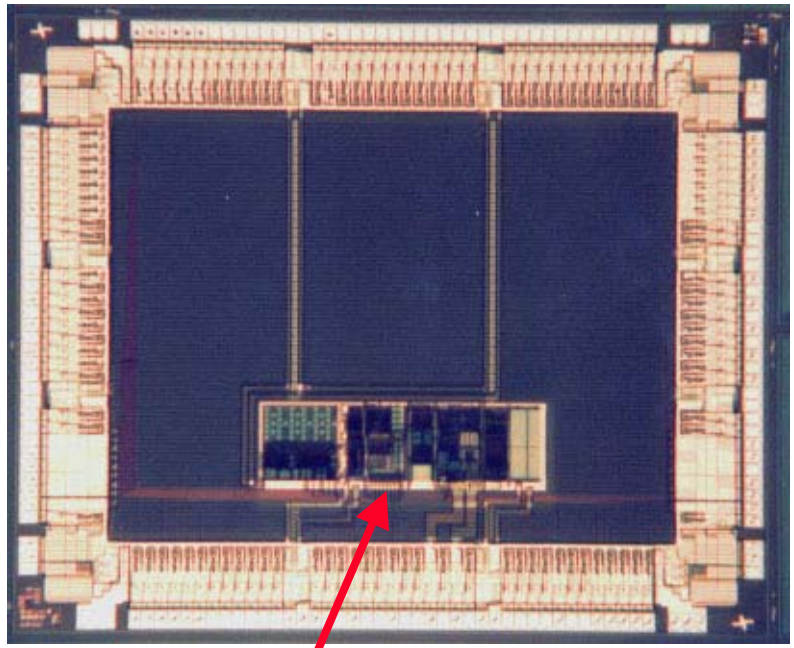
- Honeywell Has Developed 125°C Mixed-Signal ASIC Capability With U.S. Government Support (Radhard SOI4)
  - SOI 5V, 0.8μ Process *For Analog As Well As Digital*
  - Radiation Hardened For Space Applications
  - DoD Applications Will Sustain This Capability
- Mask Compatible SOI 5V, 0.8μ Process Technology Is Already Used For High-Temp. Digital Products (High Temp. SOI4)
- With Minor Modifications, The Rad-hard Space Process Can Be Applied To Commercial Down-hole
  - Adjust Transistor Threshold Parameters
  - Remove Key Radiation-hardening Steps
  - Extend Models and Libraries From 125C to 225C
  - *Adds HT Analog/Mixed-Signal Capability In 5V, 0.8μ SOI*
- Products and Design Libraries Developed For Space Market Can Be Adapted To High-Temp / Down-hole

Radhard 8-bit ADC Analog Macrocell

PARAMETER	GOAL	STATUS*
Operating Temperature	-55°C to +125°C	Tested @ 25°C and 125°C
Integral Non-Linearity	±0.5LSB	±1LSB
Diff. Non Linearity	±0.5LSB	±1LSB
Offset Error	±1LSB (10mV)	3-8mV
FS Calibration Error	0.8% of FS (typical)	0.6%
Conversion Cycle	<25µsec	Tested @ 30µsec**
Vref Out @ 25°C	2.56V ± 0.10V	2.56V ± 0.010V
Vref Out Drift w/Temp	±15mV	±5mV
Vref Out Drift w/time	±3mv/1000 hours	Not Tested
Vref Out Drift w/1MRad	TBD	-7mV after 1MRad
Vref Out Regulation	1mV/Volt	1mV/Volt

*Initial Wafer test results only, no package testing was done yet. Results should improve at package level testing.

**Oscillator was untrimmed. Can be trimmed from 10µsec to 70µsec.



8-Bit ADC Macrocell placed / Routed on Honeywell HX2040 Gate Array Underlayers

- **Successive-approximation converter with 8-bit Capacitor-DAC**
- **Built in oscillator and 2.56V buffered Voltage Reference**
- **Eight input multiplexer**
- **Separated supplies: 5V analog and 5V digital**
- **Analog macro cell for use with SOI-4 Gate Arrays**

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HW/DOE Deep-Trek Program Goals

- Operation to at least 225°C long-term, with a goal for transient excursions to 300°C
- Sustainable source for reliable down-hole micro-electronics (Silicon-on-Insulator CMOS)
  - Based on modified RH-SOI4 5V Mixed-Signal CMOS process,
- Develop key building blocks for down-hole systems
- Establish foundation for future HT development
  - Design platforms (toolkits and libraries)
- Reduce the Cost/Schedule/Risk for HT down-hole development
  - Demonstrated capabilities
  - Identify, share and support suppliers of high-temp. passives.

Summary

- SOI CMOS is widely recognized as the most viable near-term solution for extending operating temperature for integrated circuits above 175°C
- SOI CMOS is capable for analog/mixed-signal signal conditioning and control applications
- For high power-density actuator/driver applications SOI is at a disadvantage relative to SiC
- Minor modifications to SOI processes are needed to extend temperature range for complex IC's beyond 200°C
- Complete solutions are required: Analog/mixed-signal in addition to digital
- Exploiting synergy between SOI for rad-hard DoD and SOI for high-temp. down-hole applications will benefit both user communities

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